

## Safety Node

### Integration ready

#### System integrator

	Hilscher	NewTec	Wallner Automation
Evaluation board available	+ (NSFEB-M52)	+ (SafeFlex - FSDK)	+
Safety conformance level	SIL3, PL <sub>e</sub> / Cat. 4	SIL3, PL <sub>e</sub> / Cat. 4	SIL3, PL <sub>e</sub> / Cat. 4
SIL3-ready hardware (pre-certified)	+ (NSF-M52)	+ (SafeFlex - FSDK)	+
SIL3-ready software	+	+	+
IO-Interface (number, type)	3xDI with monitoring function / 1xDIO (AIDA Standard)	6xDI / 4xDIO	8xDI available, DAS and DIO on request
OSSD	Available	Available	Available
Processor	ARM	NIOS	ARM or NIOS
RAM size	8 MB SDRAM	1GB DDR3 RAM	bis 256 kB / processor
Network interface	netX52	2 FPGA (ALTERA Cyclone V)	FPGA (ALTERA Cyclone IV)
Multi-protocol ready	+	+	+
System interface	SPI	+	+
Design variants	Piggy back board	Design-In	Piggy back board, Design-In
Customer specific development	o (with MESCO)	+	+
Consulting	o (with MESCO)	+	+
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Legend: + = yes, o = no

### Customer specific development and consulting

#### System integrator

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ETHERNET  open SAFETY   
**POWERLINK SAFETY**

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MM-FO-PL-IO-EN-01  
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## Master

POWERLINK and openSAFETY nodes can be implemented as various models which differ with regard to cost and flexibility. Customers can thus choose the optimal solution for their requirements, combining maximum functionality with minimal costs.

POWERLINK master solutions can be implemented on any operating system and any hardware platform, guaranteeing full reusability of existing know-how and equipment. The open source configuration tool openCONFIGURATOR ([www.sourceforge.net](http://www.sourceforge.net)) hereby guarantees efficient configuration for this open automation solution.

POWERLINK slave interface connections can be realized as multi-protocol solutions and as POWERLINK-only interfaces in both cases using openSAFETY for safety communication.

openPOWERLINK: [www.sourceforge.net](http://www.sourceforge.net)

<b>Any operating system</b>				
<b>Any interface</b>	PCIe	Parallel	Shared memory	No-OS
<b>Any hardware platform</b>	Intel X86	FPGA	Standard Ethernet	ARM
	<b>Example design 1: Any PC</b>	<b>Example design 2: PC + additional hardware</b>	<b>Example design 3: FPGA SoC</b>	<b>Your design:</b>
<b>Operating system</b>	Linux	Windows 7 (64 Bit)	No-OS	
<b>Interface</b>	IO CTL	PCIe	SoC proprietary	
<b>Hardware platform</b>	Standard Ethernet	FPGA	FPGA	

Multi-protocol slave solutions allow for high flexibility: the component manufacturer must decide on a specific hardware platform and yet need not choose the Industrial Ethernet bus of the module until it is delivered. Choosing openSAFETY as safety protocol combined with such a multi-protocol solution reduces the safety development effort to an absolute minimum.

In a POWERLINK-only interface, all electronics can be optimized for the resource-saving POWERLINK technology, allowing users to implement a very cost-efficient Industrial Ethernet interface.

## Slave

	FPGA technology						ARM technology	netX technology	Anybus technology		
	Altera			Xilinx			example TI	Hilscher	HMS		
<b>Solution provider</b>	KUNBUS	port	B&R	Kalycito	SYS TEC electronic	Softing	port	B&R	port	Hilscher	HMS
<b>Hardware type</b>	Cyclone IV	Cyclone III, Cyclone IV	Cyclone IV	Cyclone IV	Cyclone III	Cyclone Familie	Spartan 3, Spartan 6, Virtex 4, Virtex 5, Zynq	Spartan 6	Sitara AM335X, STM32	PC-Card: dX Module: netJACK, comX, netFC, netRAPID, Chip: netX100, netX51, netX52, netX6	Brick B40, Module M40, Chip C40
<b>µC interfaces serial:</b>											
<b>UART</b>	+	o	o	o	o	o	o	o	+	+	+
<b>I2C</b>	o	o	o	o	o	o	o	o	+	+	o
<b>SPI</b>	+	+	+	+	+	+	+	+	+	+	+
<b>µC interfaces parallel:</b>											
<b>PCI</b>	o	o	o	o	o	+	o	o	+	+	o
<b>DPRAM</b>	+	+	+	+	+	+	+	+	+	+	+
<b>8 / 16 Bit</b>	+	+	+	+	+	+	+	+	+	+	+
<b>µC interface libraries</b>	o	API	CN API	n.a.	n.a.	SDAI	API	n.a.	API	o	Anybus
<b>Direct IO - support</b>	+	+	+	+	+	+	+	+	+	+	+
<b>License model</b>	ANSI-C source code, buyout, no royalties	ANSI-C source code, buyout, no royalties	Buyout	BSD-License	BSD-License		ANSI-C source code, buyout, no royalties	ANSI-C source code, buyout, no royalties	ANSI-C source code, buyout, no royalties	Slave stack license is included in chip / module price	Slave stack license is included in chip price
<b>Multi-protocol solution possible</b>	+	+	o	o	o	+	+	o	+	+	+
<b>Fastest supported cycle time (all application depending)</b>	200 µs	200 µs	200 µs	200 µs	200 µs	400 µs	200 µs	200 µs	200 µs	200 µs	200 µs
<b>Automated FW upgrade</b>	+	o	+	+	+	+	o	o	o	o	o
<b>Cross traffic</b>	+	+	+	+	+	+	+	+	+	+	+
<b>Poll Response Chaining</b>	+	o	+	+	+	+	o	+	o	o	+
<b>Multi-ASnd</b>	+	o	+	+	+	+	o	+	o	o	o
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Legend: + = yes, o = no