

NEWS

Page 1
**Meet the EPSG at
upcoming trade shows**

Page 1-2
**European Industrial
Ethernet Award**

Page 2-4
**How to implement a
POWERLINK interface
on your device**

Page 5
**Open, simple and more
cost-efficient than ASIC
solutions: POWERLINK
interface connection
from port**

Page 6
**CANopen and POWERLINK
now also available as X67
High Density Bus Controller**

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Meet the EPSG at upcoming trade shows

The EPSG invites all interested parties to its booth at upcoming automation trade shows. The POWERLINK user organization will be an exhibitor (Hall 6, Booth 114) at this year's SPS/IPC/DRIVES, which will take place from November 25-27 in Nuremberg, Germany. The SCS (Systèmes, Composants et Solutions) trade show, which will take place from December 2-5 in Paris, France, is another opportunity to learn about POWERLINK - the EPSG will be present in booth 6.J.051. We are looking forward to your visit!

EPSG at SPS/IPC/DRIVES: Tuesday, Nov. 25, 2008 - Thursday, Nov. 27, 2008
Nuremberg, Germany Hall/Booth: 6/114

EPSG at SCS: Tuesday, Dec. 02, 2008 - Friday, Dec. 05, 2008
Paris, France Hall/Booth: 6.J.051

European Industrial Ethernet Award

Announcing the European Industrial Ethernet Award, the company B&R invites students to participate in the first pan-European university competition of its kind.



Figure: B&R calls for innovative, creative projects and solutions integrating POWERLINK technology

B&R calls for innovative concepts, creative solutions, practice-oriented application suggestions and promising scientific research projects from all technical disciplines.

continued on next page →

NEWS

Page 1
**Meet the EPSG at
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continued: **European Industrial Ethernet Award**

The only requirement for your proposal is the usage of POWERLINK technology in any form. The freely available open source software openPOWERLINK can be used as an ideal basis for an optional practical implementation.

A high-profile jury of researchers and economic experts will assess all submitted projects and announce the award winners in mid-2009. The winners will be awarded three attractive main prizes worth 10,000, 5,000 and 2,500 Euro.

openPOWERLINK is the only open source real-time protocol solution based on standard-compliant Ethernet. openPOWERLINK's source code has been made freely available. In addition to that, the open source license model (BSD license) allows for unlimited adaptation and use of the software in user applications. Thereby, applications with high requirements on timing precision and dynamic reactions can be easily and cost-efficiently realized.

Further information is available from:
<http://www.br-automation.com/award>
<http://www.sourceforge.net/projects/openPOWERLINK>

How to implement a POWERLINK interface on your device

“How can I implement a POWERLINK interface for my application?” is one of the questions asked by manufacturers and fieldbus operators who have already witnessed the protocol's advantages. In the following, we will briefly address central questions concerning POWERLINK Master and Slave solutions as well as their individual performance and advantages.

POWERLINK can generally be integrated into any standard Ethernet design irrespective of the choice of processor architecture, either as a single-processor solution or with co-processor support. For single processor solutions, POWERLINK is directly integrated on the application processor, and uses a standard Ethernet controller as its bus connection. Open source versions of the POWERLINK Master and Slave stacks are available as free-of-charge downloads for Linux and Windows XP operating systems. openPOWERLINK for Linux is available from sourceforge.net/projects/openpowerlink, and openPOWERLINK for Windows XP can be downloaded from kalycito.com/downloads.html#powerlinkxp.

continued on next page →

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Page 1
**Meet the EPSG at
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Page 1-2
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Ethernet Award**

Page 2-4
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POWERLINK interface
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POWERLINK Master

POWERLINK can be used without hardware support on any operating system of choice, e.g. Windows, Linux, or VxWorks, with a standard onboard Ethernet controller. The jitter and cycle times that can be achieved are contingent on CPU performance and the accuracy of the operating system. Cycle times around 500 μ s and jitter values of about 30 μ s are typical. Integrating a PCI card with a POWERLINK pre-implementation into the system is an alternative option for a POWERLINK Master. In this case, a co-processor handles the protocol stack and saves central processor resources. Cycle times reach 100 μ s with an accuracy of 0.1 μ s.

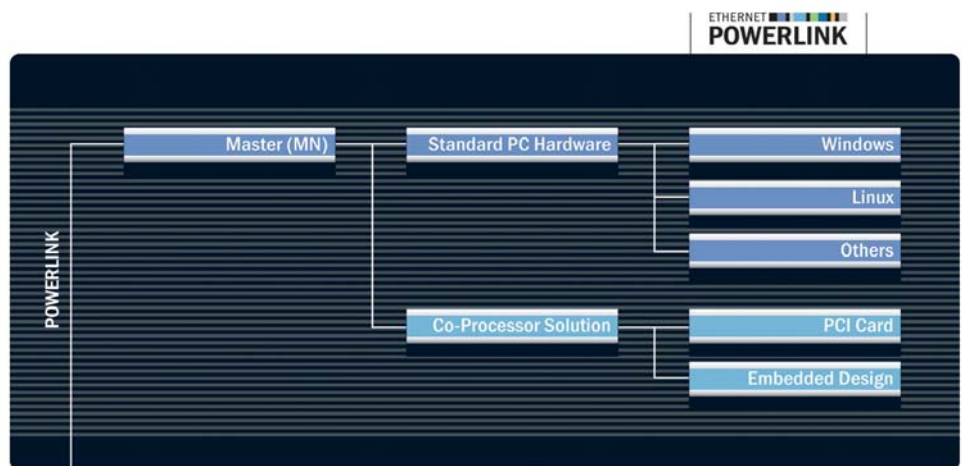


Figure 1: Implementation options for the Managing Node (Master)

POWERLINK Slave

Likewise, POWERLINK Slaves can be implemented as stacks on the application processor, or alternatively be based on dedicated communication hardware. POWERLINK Slave implementation types range from ready-to-run evaluation boards or piggyback-style single boards, which are suitable for prototyping or for series manufacturing of smaller lots, to optimized, FPGA-based chip solutions complete with the protocol as well as the application software. These various options differ in terms of flexibility as well as cost. Multi-protocol solutions allow component manufacturers to use a consistent hardware platform that is open for various Industrial Ethernet solutions, and only calls for a decision for a specific fieldbus when a product is customized to be shipped to an end user. This option is usually more expensive than dedicated POWERLINK only solutions. Multi-protocol ASICs accommodate the entire system design in one chip. Benefits include the defined interface between the communication processor and application processor, but there are also drawbacks such as the fixed programming interface, and higher hardware costs, or costs that vary with production lots. Multi-protocol FPGA solutions also provide flexibility for environments where different protocols are used. In contrast to ASIC solutions, users have an influence on the API and gain

continued on next page →

NEWS

Page 1
Meet the EPSG at upcoming trade shows

Page 1-2
European Industrial Ethernet Award

Page 2-4
How to implement a POWERLINK interface on your device

Page 5
Open, simple and more cost-efficient than ASIC solutions: POWERLINK interface connection from port

Page 6
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continued: **How to implement a POWERLINK interface on your device**

more flexibility. However, they should be aware that the hardware costs are contingent on the resource requirements of the most demanding protocol involved. POWERLINK-only FPGA solutions provide more economic alternatives, and are flexible regarding the interface. Conventional 32-bit CPUs equipped with internal RAM and internal flash memory constitute the most cost-efficient option to connect a Slave, clearly undercutting even the price range of other, ASIC-based protocols, while still ensuring that users enjoy the flexibility and openness of a standard microprocessor. A common characteristic of all options is that they feature a flexible connection of the application and communication software, e.g. via dual port RAM or a serial interface.

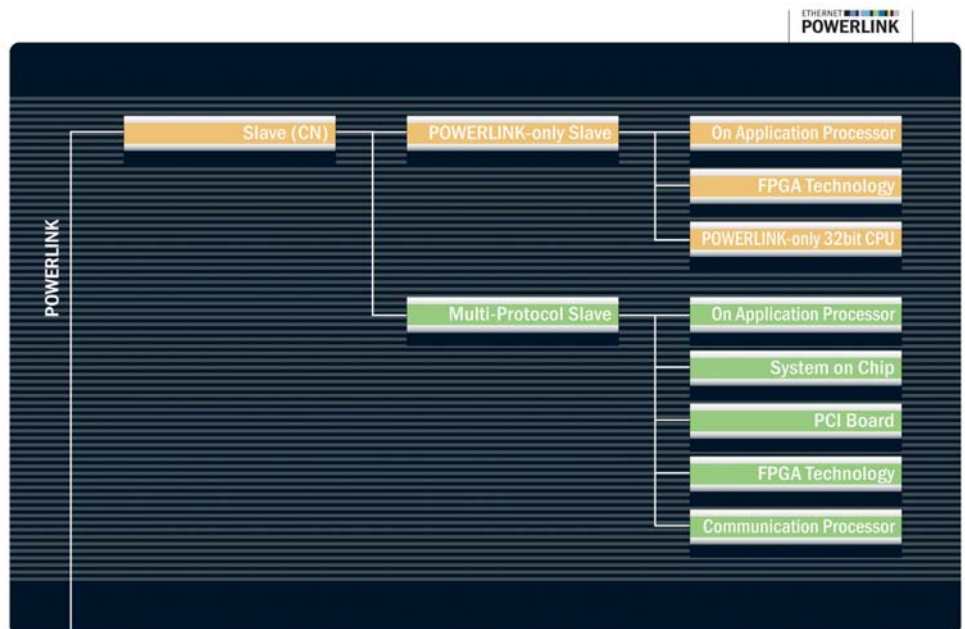


Figure 2: Implementation options for the Controlled Node (Slave)

Interested parties with a background in CANopen wishing to learn more about POWERLINK implementation can approach their CANopen service providers. The POWERLINK office will, of course, also arrange individual consulting for all questions.

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**100% open
technology**

- no license fees
- no patents
- technology not owned by single persons or companies
- POWERLINK users are not obligated to become members of any association or to sign any contract
- independence from ASIC providers
- open source software for masters and slaves

NEWS

Page 1
Meet the EPSG at upcoming trade shows

Page 1-2
European Industrial Ethernet Award

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Open, simple and more cost-efficient than ASIC solutions: POWERLINK interface connection from port

port provides a high-performance, cost-efficient and open solution which allows users to connect devices to POWERLINK networks. The systems house for CAN, CANopen and real-time Ethernet automation solutions has adapted a POWERLINK stack to the architecture of STMicroelectronics' STR912FA microcontroller.

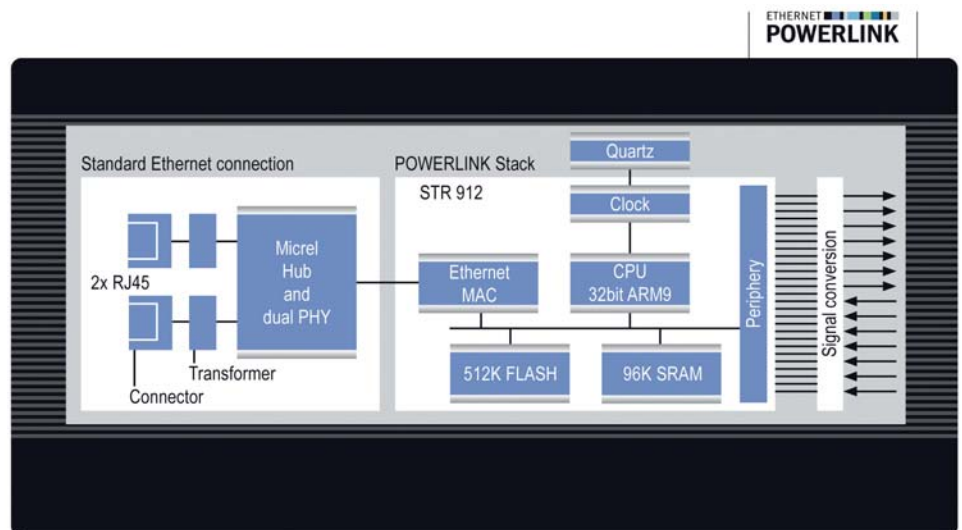


Figure: Diagram of the STR912FA-based connection

The microcontroller unit combines a 32 bit ARM9 CPU, 96 kB SRAM, flash storage capacity between 512 kB and 2.1 MB, an Ethernet controller and a real-time clock. The solution ensures response times below 5 μ s. *port*'s stack and ST's hardware allow users to implement a POWERLINK connection for their devices which requires few components, with overall costs below those of an ASIC-based solution. If the MCU is equipped with a larger flash memory, users can also implement a multi-protocol design, thus enabling connections to all software-based protocols such as Ethernet/IP, Modbus TCP or Profinet IO and RT. In order to adapt the solution for CANopen and DeviceNet networks, users merely need to connect a CAN transceiver. *port* supports manufacturers with further products which facilitate development, such as a design tool which enables the fast compilation of object dictionaries and output of EDS files, and a starter kit containing all components required to develop a prototype as well as sample applications and an analyzer which measures specific time values. The solution comes with a wide range of helpful tools: the JTAG-capable hardware, for example, ensures efficient debugging. Moreover, manufacturers are free to use the free-of-charge GNU compiler collection (GCC).

NEWS

Page 1
**Meet the EPSG at
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Page 1-2
**European Industrial
Ethernet Award**

Page 2-4
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POWERLINK interface
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cost-efficient than ASIC
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CANopen has become one of the leading I/O profile standards in the automation industry. Originally designed solely for CAN, it can now also be found in other forms. Particularly in combination with POWERLINK, it expands into the high-performance realm with real-time Ethernet.

New bus controllers have been introduced for both CAN and POWERLINK to round off the existing range of products.

The CAN bus controller meets the CANopen specifications DS 301 and DS 401. Automatic baud rate detection, PDO linking, life/node guarding, emergency objects and many more features are supported. The integrated X2X Link connection makes it possible to connect additional modules. AutoMapping is used to automatically detect these modules, whose data is then placed in the I/O map. 16 digital channels can be configured to operate as digital inputs or outputs, which are then individually directed to M8 connections.



Figure: X67 High Density Bus Controller for POWERLINK

The POWERLINK bus controller, also designed with IP67 protection, has two M12 connections for the fieldbus to allow easy network wiring. An additional M12 serves as the connection for expansion modules. 16 additional digital channels are also provided here, which can each be configured to operate as input or output. Depending on the design, these are directed individually to M8 or in pairs to M12 connections.

Both systems provide the user considerable cost savings by offering an integrated T-connector/integrated hub. The integrated connection for local expansion makes it possible to connect any system component from the B&R series X20, X67 and XV.

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Masthead:

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